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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,969	10/11/2001	David W. Boerstler	AUS920010608US1	8113

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04/18/2003

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EXAMINER

KINKEAD, ARNOLD M

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 04/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/974,969

Applicant(s)

BOERSTLER ET AL.

Examiner

Arnold M Kinkead

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

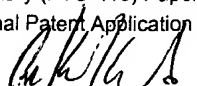
Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: 

Art Unit: 2817

DETAILED ACTION

Please submit all related serial numbers

Claim Objections

1. Claim 20 is objected to because of the following informalities: The claim dependency should be corrected to be from a lower numbered claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5,6,13,14,21,22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards claims 5,6,13,14,21, and 22 , accordingly, recite “ a third PFET” and “ a third NFET” , with corresponding “ fifth drain...fifth source ...and fifth gate terminal” however, there is no previous recitation for a first and second PFET and a first and second NFET...

Art Unit: 2817

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-4, and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao(US 5,418,499) in view of Leonowich (US 5,434,525) and further in view of Chow et al(US 5,815,043).

The reference by Nakao discloses a multi-mode VCO, see figure14, for example, comprising a ring oscillator with an odd number($N \geq 3$) of delay stages(logic inverter gates, $G1-Gn$). Forward conduction circuit(s) are shown(TF11, IG11...) with first input and output(nodes coupling output of $G3$ and $G1$) and control inputs being the gate terminals of TF11. This forward conduction circuit comprises a bi-directional conduction circuit(transfer gate, TF11, with third input and third output); the control inverter(IG11) has the

Art Unit: 2817

second input and second output. The bi-directional element is comprised of a first PMOS and a first NMOS devices with the conventional S,D, coupling. The coupled drain terminals being coupled to the third input terminal, and the source terminals coupled to the third output terminal. The control signal(SF,SF_) are coupled to the first and second gates, respectively. The forward conduction circuits are coupled in parallel with a selected number of logic inverter gates by way of the control signals.

The reference does not disclose a selectable inverter circuit coupled in parallel to each of the inverter stages with selectable logic inverter gate, first electronic switch and second electronic switch. The references by Leonowich and Chow et al will serve to highlight these conventional elements. With regards the use of parallel connected inverter gates coupled across the ring oscillator delay stages, the reference by Leonowich discloses a PLL(see figure 5) with differential phase detector and inherent charge pump output signals(albeit not shown) coupled to the ring oscillator(see figure 1) to allow for the frequency control as desired(via VCN,VCP mode control signals), note, inherently, there will be intrinsic capacitances and ultimately delay stage capacitance on each pump out line. The reference makes use of parallel connected inverters to vary the frequency of the ring oscillator. Note that the electronic switches will include the inverter (14, with MOSFET switches coupled between rails(first and second power supply voltages.)

The Leonowich reference is silent on a selectable inverter circuits, and the reference by Chow et al is relied upon for suggesting that the parallel connected inverter circuits may indeed be selectable, i.e., via the transfer gates(see figures 7 and 8). The reference by Chow et al discloses a computer system with controlled ring oscillator within a PLL, that includes a CPU(202),DRAM(204), data bus(I/O), etc. this inherently includes access to EPROMS/ ROM devices all of which are synchronized by way of a clock signal

Art Unit: 2817

from the PLL VCO(see figure 2 and 4). In figures 4, 7, and 8, selecting a particular transfer gate to increase/decrease the frequency is achieved and each gate is coupled in parallel with a respective inverter stage.

In light of the above it would have been obvious to one of ordinary skill in the art to have modified the reference by Nakao to include selectable inverter circuits , as suggested by Leonowich and Chow et al taken together, comprising inverters in parallel to each delay logic inverter gate with selection means as highlighted in Chow and thus achieve enhanced frequency adjustment. Both the Leonowich and Chow et al references suggesting that this parallel arrangement allows for this increased frequency flexibility.

6. Claims 9-12, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al(US 5,815,043)) in view of Nakao(US 5,418,499)and further in view of Leonowich (US 5,434,525) .

The reference by Chow et al discloses a computer system with controlled ring oscillator within a PLL, that includes a CPU(202),DRAM(204), data bus(I/O), etc. this inherently includes access to EPROMS/ ROM devices all of which are synchronized by way of a clock signal from the PLL VCO(see figure 2 and 4). In figures 4, 7, and 8, selecting a particular transfer gate to increase/decrease the frequency is achieved and each gate is coupled in parallel with a respective inverter stage.

The reference does not disclose forward conduction circuits with bi-directional and control inverter circuits, to control the number of stages within the loop, and ultimately, the frequency, which is a conventional idea in ring oscillators; also, an inverter is not shown with the transfer gate for coupling across individual ring delay stages.

Art Unit: 2817

The reference by Nakao discloses a multi-mode VCO, see figure 14, for example, comprising a ring oscillator with an odd number ($N \geq 3$) of delay stages (logic inverter gates, $G1-Gn$). Forward conduction circuit(s) are shown (TF11, IG11...) with first input and output (nodes coupling output of $G3$ and $G1$) and control inputs being the gate terminals of TF11. This forward conduction circuit comprises a bi-directional conduction circuit (transfer gate, TF11, with third input and third output); the control inverter (IG11) has the second input and second output. The bi-directional element is comprised of a first PMOS and a first NMOS devices with the conventional S,D, coupling. The coupled drain terminals being coupled to the third input terminal, and the source terminals coupled to the third output terminal. The control signal (SF, SF_) are coupled to the first and second gates, respectively. The forward conduction circuits are coupled in parallel with a selected number of logic inverter gates by way of the control signals.

With regards the use of parallel connected inverter gates coupled across the ring oscillator delay stages, the reference by Leonowich discloses a PLL (see figure 5) with differential phase detector and inherent charge pump output signals (albeit not shown) coupled to the ring oscillator (see figure 1) to allow for the frequency control as desired (via VCN, VCP mode control signals), note, inherently, there will be intrinsic capacitances and ultimately delay stage capacitance on each pump out line. The reference makes use of these parallel connected inverters to vary the frequency of the ring oscillator.

In light of the above it would have been obvious for one of ordinary skill in the art to have modified the Chow et al ring oscillator to include the inverter circuit in the selectable transfer gate path to control the current that is used to increase/decrease the frequency of the oscillator as noted in Leonowich. Also, modifying the oscillator of Chow et al to include the forward conduction circuit as described by Nakao above,

Art Unit: 2817

also allows for further frequency control in allowing the number of delay stages to be changed and thus the frequency of oscillation is changed.

7. Claims 17-20, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leonowich (US 5,434,525) in view of Nakao(US 5,418,499) and further in view of Chow et al(US 5,815,043)

Leonowich discloses a PLL(see figure 5) with differential phase detector and inherent charge pump output signals(albeit not shown) coupled to the ring oscillator(see figure 1) to allow for the frequency control as desired(via VCN,VCP mode control signals), note, inherently, there will be intrinsic capacitances and ultimately delay stage capacitance on each pump out line. The reference makes use of these parallel connected inverters circuits(14,15) to vary the frequency of the ring oscillator.

The reference by Leonowich does not suggest ring oscillator circuit with conventional forward conduction circuit nor a selectable inverter circuit. Also, no divider is shown in the feedback loop.

With regards the VCO output divider, this is a conventional element for PLL' s and serves to allow frequency adjustment of the VCO as desired.

With regards the forward conduction circuit, the reference by Nakao is relied upon to show that this allows enhanced frequency control. The reference by Nakao discloses a multi-mode VCO, see figure14, for example, comprising a ring oscillator with an odd number($N \geq 3$) of delay stages(logic inverter gates,G1-Gn). Forward conduction circuit(s) are shown(TF11,IG11...) with first input and output(nodes coupling output of G3 and G1) and control inputs being the gate terminals of TF11. This forward conduction circuit comprises a bi-directional conduction circuit(transfer gate,TF11, with third input and third output); the control

Art Unit: 2817

inverter(IG11) has the second input and second output. The bi-directional element is comprised of a first PMOS and a first NMOS devices with the conventional S,D, coupling. The coupled drain terminals being coupled to the third input terminal, and the source terminals coupled to the third output terminal. The control signal(SF,SF_) are coupled to the first and second gates, respectively. The forward conduction circuits are coupled in parallel with a selected number of logic inverter gates by way of the control signals.

With regards the use of a selectable inverter circuit, the reference by Chow et al is relied upon. The reference by Chow et al discloses a computer system with controlled ring oscillator within a PLL, that includes a CPU(202),DRAM(204), data bus(I/O), etc. this inherently includes access to EPROMS/ ROM devices all of which are synchronized by way of a clock signal from the PLL VCO(see figure 2 and 4). In figures 4, 7, and 8, selecting a particular transfer gate to increase/decrease the frequency is achieved and each gate is coupled in parallel with a respective inverter stage. This allows for enhanced frequency control as well.

In light of the above it would have been obvious to one of ordinary skill in the art to have modified the PLL circuit of Leonowich to include conventional frequency control means such as the output divider for dividing the VCO output as desired as well as the forward conduction circuit as noted above by Nakao to allow for enhanced frequency control. The implementation of selectable transfer gate/inverter circuit is shown by Chow et al also enhancing the frequency of the VCO.

Art Unit: 2817

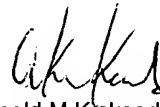
Allowable Subject Matter

With regards the claims rejected under 112, 2nd paragraph the examiner will consider the allowableness of the corrected claims when the applicant responds.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 703-305-3486. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 703-308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
April 15, 2003